

# **OKI Semiconductor MR27V6402G**

Oki	Network Solutions
<u> </u>	Network Colutions
	for a Global Society

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## 4M–Word $\times$ 16–Bit or 8M–Word $\times$ 8–Bit OTP

### **GENERAL DESCRIPTION**

The MR27V6402G is a 64 Mbit electrically One Time Programmable Read-Only Memory that can be electrically switched between 4,194,304-word х 16-bit and 8,388,608-word  $\times$  8-bit by the state of the BYTE# pin. The MR27V6402G supports high speed asynchronous read operation using a single 3.3V power supply.

### **FEATURES**

 $\cdot$  4,194,304-word  $\times$  16-bit / 8,388,608-word  $\times$  8-bit electrically switchable configuration

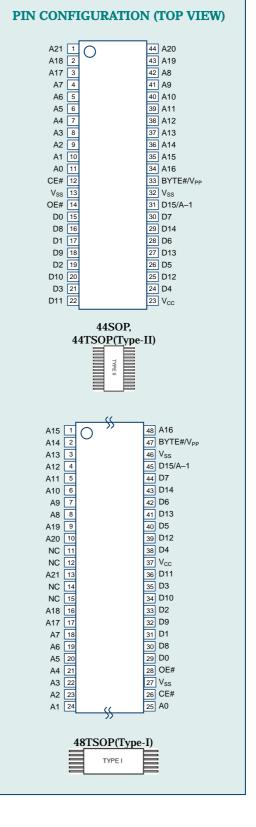
- $\cdot$  +3.0 V to 3.6 V power supply 80 ns MAX
- · Access time
- · Operating current 20 mA MAX (5MHz)
- · Standby current 10 µA MAX
- · Input/Output TTL compatible
- · Three-state output

### PACKAGES

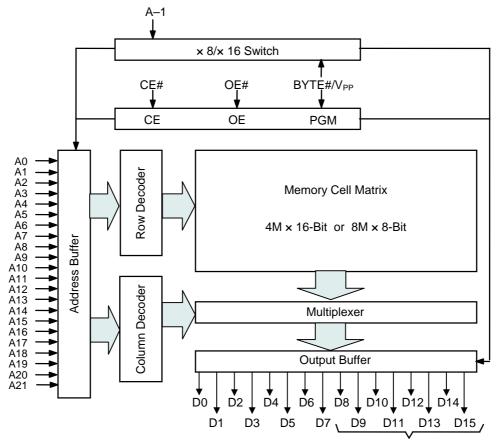
- · MR27V6402GMA
- 44-pin plastic SOP (SOP44-P-600-1.27-K)
- · MR27V6402GTP

44-pin plastic TSOP (TSOP II 44-P-400-0.80-K) · MR27V6402GTN

48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)



#### **BLOCK DIAGRAM**



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

#### **PIN DESCRIPTIONS**

Pin name	Functions
D15 / A–1	Data output / Address input
A0 to A21	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#/V <sub>PP</sub>	Mode switch/Program power supply voltage
Vcc	Power supply voltage
V <sub>SS</sub>	Ground
NC	No connect

### **FUNCTION TABLE**

Mode	CE#	OE#	BYTE#/V <sub>PP</sub>	V <sub>CC</sub>	D0 to D7	D8 to D14	D15/A–1
Read (16-Bit)	L	L	Н			D <sub>OUT</sub>	
Read (8-Bit)	L	L	L	2.0.1/	D <sub>OUT</sub>	Hi–Z	L/H
Output disable	1	ц	Н	3.0 V		Hi–Z	
	L	Н	L	to 3.6 V		n-z	*
Chandley	Н	*	н	3.0 V		11: 7	
Standby			L			Hi–Z	*
Program	L	Н				D <sub>IN</sub>	
Program inhibit	Н	Н	V <sub>PP</sub>	Vcc		Hi–Z	
Program verify	H	L	]			D <sub>OUT</sub>	

\*: Don't Care (H or L)

### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	—	-55 to 125	°C
Input voltage	VI		–0.5 to V <sub>CC</sub> +0.5	V
Output voltage	Vo	relative to Vss	–0.5 to V <sub>CC</sub> +0.5	V
Power supply voltage	Vcc		–0.5 to 5	V
Program power supply voltage	V <sub>PP</sub>		-0.5 to 11.5	V
Power dissipation per package	PD	_	1.0	W

### **RECOMMENDED OPERATING CONDITIONS**

					(Ta	= 0 to 70°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V <sub>CC</sub> power supply voltage	V <sub>cc</sub>		3.0	—	3.6	V
V <sub>PP</sub> power supply voltage	V <sub>PP</sub>	$V_{\rm CC} = 3.0$ to 3.6 V	-0.5	—	V <sub>CC</sub> +0.5	V
Input "H" level	VIH	$v_{\rm CC} = 3.0 10 3.0 V$	2.2	—	V <sub>CC</sub> +0.5*	V
Input "L" level	VIL		-0.5**	—	0.6	V

Voltage is relative to V<sub>SS</sub>.

\* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

### **PIN CAPACITANCE**

#### (V<sub>CC</sub> = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C <sub>IN1</sub>	$V_1 = 0 V$	—	—	8	
BYTE#/V <sub>PP</sub>	C <sub>IN2</sub>	$v_1 = 0 v$	_	_	200	pF
Output	C <sub>OUT</sub>	$V_0 = 0 V$	—	—	10	

### **ELECTRICAL CHARACTERISTICS**

#### **DC Characteristics**

$(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, \text{ Ta} = 0 \text{ to } 70$						
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_1 = 0$ to $V_{CC}$	_	_	10	μA
Output leakage current	I <sub>LO</sub>	$V_{O} = 0$ to $V_{CC}$	_	_	10	μA
V <sub>CC</sub> power supply current	Iccsc	$CE\# = V_{CC}$	_	_	10	μA
(Standby)	I <sub>CCST</sub>	$CE\# = V_{IH}$	_	_	1	mA
V <sub>CC</sub> power supply current (Read)	I <sub>CCA</sub>	$CE\# = V_{IL}, OE\# = V_{IH}$ f=5MHz	—	—	20	mA
V <sub>PP</sub> power supply current	I <sub>PP</sub>	$V_{PP} = V_{CC}$	_	_	10	μA
Input "H" level	VIH	—	2.2	_	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>	—	-0.5**	_	0.6	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> = –2mА	2.4	_	_	V
Output "L" level	V <sub>OL</sub>	$I_{OL} = 4mA$			0.4	V

Voltage is relative to V<sub>SS</sub>.

\* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

#### **AC Characteristics**

	$(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, \text{ Ta} = 0 \text{ to } 7$						
Parameter	Symbol	Condition	Min.	Max.	Unit		
Address cycle time	t <sub>C</sub>	—	80	_	ns		
Address access time	t <sub>ACC</sub>	$CE\# = OE\# = V_{IL}$		80	ns		
CE# access time	t <sub>CE</sub>	$OE\# = V_{IL}$		80	ns		
OE# access time	t <sub>OE</sub>	$CE\# = V_{IL}$		30	ns		
Output disable time	t <sub>CHZ</sub>	$OE\# = V_{IL}$	0	20	ns		
	t <sub>OHZ</sub>	$CE\# = V_{IL}$	0	20	ns		
Output hold time	t <sub>OH</sub>	$CE\# = OE\# = V_{IL}$	0		ns		

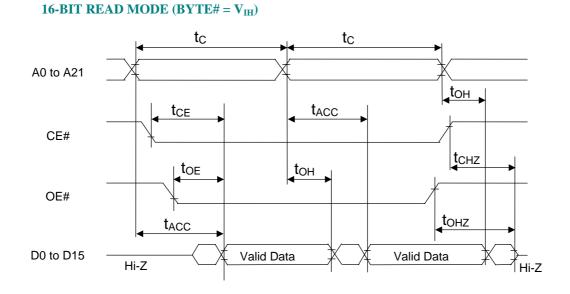
Measurement conditions

Input signal level0	V/3 V
Input timing reference level1,	/2Vcc
Output load5	0 pF
Output timing reference level 1/	/2Vcc

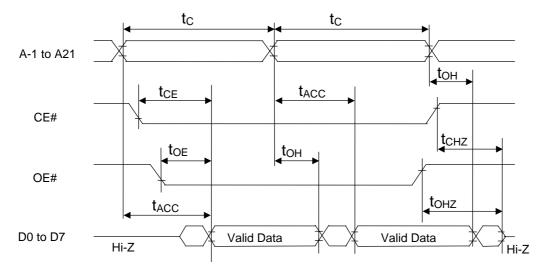
#### Output load

Output	•	
	Ī	50 pF (Including scope and jig)

### TIMING CHART (READ CYCLE)



8-BIT READ MODE (BYTE $\# = V_{IL}$ )



### ELECTRICAL CHARACTERISTICS (PROGRAMMING OPERATION)

#### **DC CHARACTERISTICS**

					(Ta = 2	5°C ± 5°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = V_{CC}$ +0.5 V	—		10	μA
V <sub>PP</sub> power supply current (Program)	I <sub>PP2</sub>	$CE\# = V_{IL}$	—		50	mA
V <sub>CC</sub> power supply current	Icc	—	—		50	mA
Input "H" level	V <sub>IH</sub>	—	V <sub>CC</sub> -0.5		V <sub>CC</sub> +0.5	V
Input "L" level	VIL	—	-0.5		0.8	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4		_	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	—		0.45	V
Program voltage	V <sub>PP</sub>	_	8.0	8.2	8.4	V
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	—	3.9	4.0	4.1	V

Voltage is relative to V<sub>SS</sub>.

### AC CHARACTERISTICS

(V <sub>CC</sub> = 4.0 V ± 0.1 V, BYTE#/V <sub>PP</sub> = 8.2 V ± 0.25 V, Ta = 25°C ± 5°C						$5^{\circ}C \pm 5^{\circ}C$ )
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Address set-up time	t <sub>AS</sub>	—	100	_	—	ns
OE# set-up time	t <sub>OES</sub>	—	2	_	—	μs
Data set-up time	t <sub>DS</sub>	—	100	_	—	ns
Address hold time	t <sub>AH</sub>	_	2	_	—	μs
Data hold time	t <sub>DH</sub>	—	100	—	—	ns
Output float delay time from OE#	t <sub>OHZ</sub>	—	0	_	100	ns
V <sub>PP</sub> voltage set-up time	t <sub>VS</sub>	_	2	_	—	μs
Program pulse width	t <sub>PW</sub>	—	7	8	9	μs
Data valid from OE#	t <sub>OE</sub>	—		_	100	ns
Address hold from OE# high	t <sub>AOH</sub>	_	0	_	—	ns

#### **Pin Check Function**

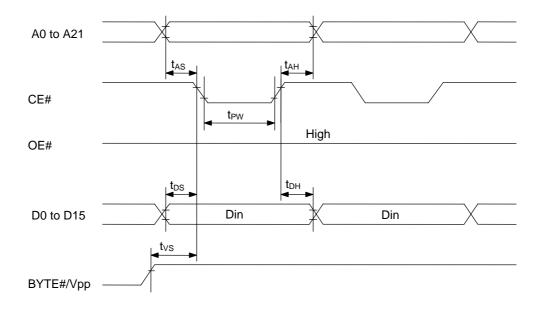
Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer. Setting up address as following condition call the preprogrammed codes on device outputs.

									×±00)													
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	DATA
0	1	0	1	0	1	0	1	0	VH	0	1	0	1	0	1	0	0	1	1	0	0	FF00
1	0	1	0	1	0	1	0	1	VH	1	0	1	0	1	0	1	1	0	0	1	1	00FF
Other conditions										FFFF												

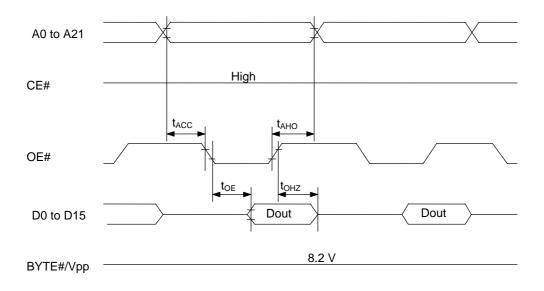
 $(V_{CC} = 3.0 \text{ V} \pm 0.1 \text{ V}, CE\# = \text{VIL}, OE\# = \text{VIL}, BYTE\#/V_{PP} = V_{IH}, Ta = 25^{\circ}C \pm 5^{\circ}C)$ 

\*: VH = 7 V ± 0.25 V

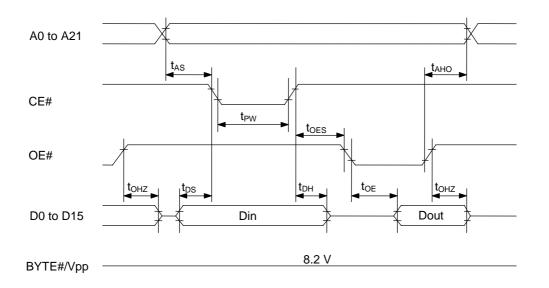
### **Consecutive Programming Waveforms**



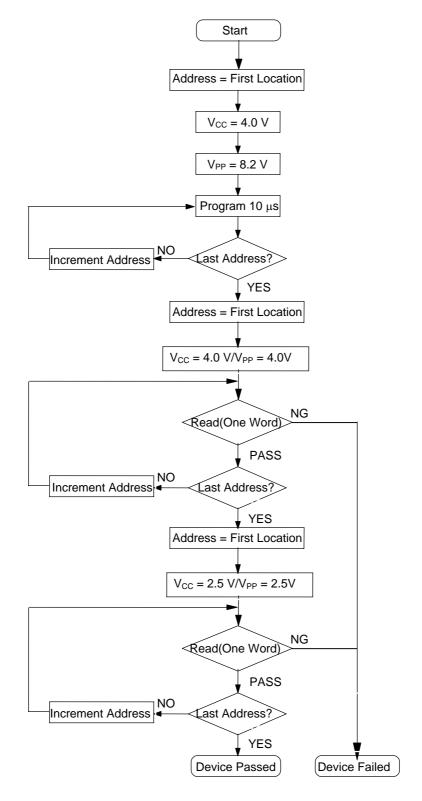
### **Consecutive Program Verify Waveforms**



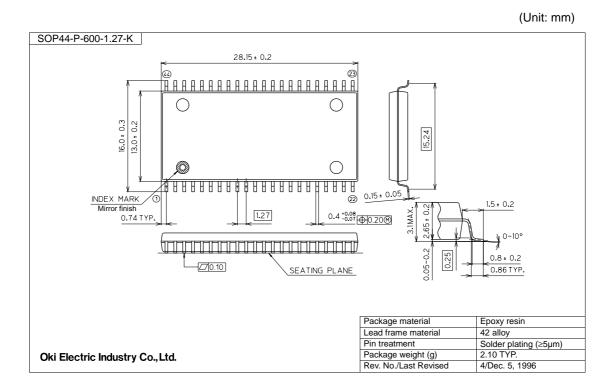
### Program and Program Verify Cycle Waveforms



#### **Programming Flow Chart**



### PACKAGE DIMENSIONS

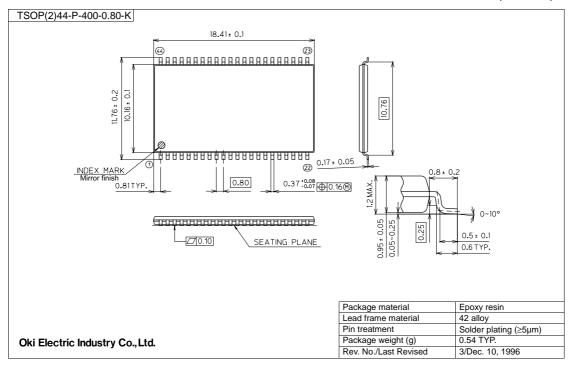


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

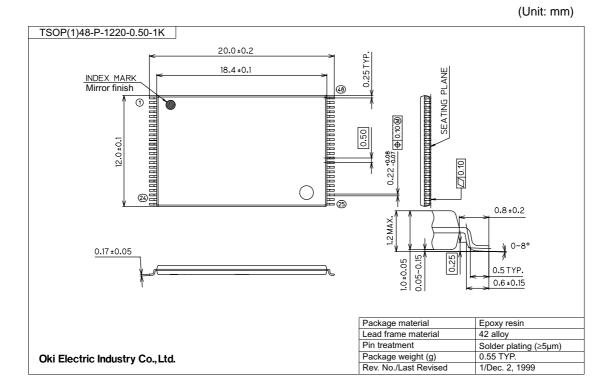




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### **REVISION HISTORY**

Document		Pa	ge					
No.	Date	Previous Edition	Current Edition	Description				
FEDR27V6402G-01-01	Apr., 2003	-	-	Final edition 1				
		1	1	Change 48TSOP(1) package code to -1K				
FEDR27V6402G-01-02	Jun 4, 2003	1, 4	1, 4	Unify Icca condition into f=5MHz				
		4	4	Change t <sub>CHZ</sub> , t <sub>OHZ</sub> to 20ns				

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